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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/764,137	01/19/2001	Yoshihito Ochi	49657-911	8210

7590 09/20/2004

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
ROSALES HANNER, MORELLA I	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/764,137	OCHI ET AL.	
	Examiner	Art Unit	
	Morella I Rosales-Hanner	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 -20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/19/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. **Claims 1 – 20** have been examined and are pending.

Information Disclosure Statement

2. The information disclosure statement (IDS) filed January 19th, 2001 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. The IDS has been placed in the application file, but the information referred to therein has not been considered.

Drawings

3. **Figures 2, 3 and 5** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Regarding claims **1 - 20**, the term "**unnecessary**" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.1 **Claims 1 – 20** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **U.S. Patent No. 6,009,249** issued to Larren Gene Weber, hereafter referred to as *Weber*.

5.1.1 As regard to **Claim 1**, this claim is drawn to a circuit simulating apparatus analyzing a circuitry having a for simulating a portion of a circuit design, comprising:

- a netlist extracting unit extracting a netlist from a circuit diagram data;
- a designating unit designating an element between the portion of the circuit to be simulated and the portion of the circuit that will be ignored;
- a circuit disconnecting unit forming a netlist with the portion of the circuit that will be ignored disconnected, from the netlist extracted by said netlist extracting unit, based on the element designated by said designating unit;

- a simulation input file forming unit forming a simulation input file, with reference to the netlist formed by said circuit disconnecting unit, a model parameter and an analysis condition; **and**
- a circuit simulating unit performing a circuit simulation using the simulation input file formed by said simulation input file forming unit.

Per independent **claim 1**: *Weber* teaches [**Col 1, line 65 – Col 2, line 7**] a system for simulating portions of a circuit design, comprising:

- a netlister tool [**Col 3, lines 45 – 67**] for extracting a netlist from a circuit diagram data;
- an unit [**Col 6, lines 53 – 67**] for designating an element between the portion of the circuit to be simulated and the portion of the circuit that will be ignored;
- a hierarchical netlister [**Col 3, lines 45 – 67**] forming a netlist with the portion of the circuit that will be ignored disconnected, from the netlist extracted by said netlist extracting unit, based on the element designated by said designating unit;
- an automated simulation circuit loader [**Col 4, lines 50 – 64**] for forming a simulation input file, with reference to the netlist formed by said circuit disconnecting unit, a model parameter and an analysis condition; **and**
- a circuit simulator [**Col 3, lines 45 - 59**] for performing a circuit simulation using the simulation input file formed by said simulation input file forming unit.

5.1.2 As regard to **Claim 2**, this claim is drawn to the circuit simulating apparatus according to claim 1, wherein:

- said designating unit includes an indicator for ignoring a portion of a circuit; **and**
- said circuit disconnecting unit forms the netlist with the portion of the circuit that will be ignored disconnected from the netlist extracted by said netlist extracting unit, based on the circuit disconnecting element designated by said circuit disconnecting terminal designating unit.

Weber teaches **[Col 3, lines 23 – 32]** the use of the "hspLoad" directive as an indicator for ignoring a portion of a circuit; and the HNL netlister **[Col 3, lines 45 – 65]**.

5.1.3 As regard to **Claim 3**, this claim is drawn to the circuit simulating apparatus according to claim 2, further comprising a circuit recognizing unit recognizing whether the circuit disconnecting terminal designated by said circuit disconnecting terminal designating unit is on the main circuit side or the portion of the circuit that will be ignored; wherein said circuit disconnecting unit adds a description for connecting the circuit disconnecting terminal recognized to be on the side of the portion of the circuit that will be ignored by said circuit recognizing unit to a power supply or to the ground, and adds a description for disconnecting connection with said portion of the circuit to be ignored, on the netlist extracted by said netlist extracting unit.

Weber teaches **[Fig 9 and corresponding text]** a PrintInstance unit that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

5.1.4 As regard to **Claim 4**, this claim is drawn to the circuit simulating apparatus according to claim 2, further comprising a circuit recognizing unit for recognizing whether the circuit disconnecting terminal designated by said circuit disconnecting terminal designating unit is on the main circuit side or on the portion of the circuit to be ignored side; wherein said circuit disconnecting unit adds a description for disconnecting connection between the circuit disconnecting terminal on the main circuit side with the circuit switching element on the netlist extracted by said netlist extracting unit, when the circuit disconnecting terminal recognized to be on the side of the main circuit by said circuit recognizing unit is connected to a plurality of elements of the main circuit.

Weber teaches **[Fig 9 and corresponding text]** a PrintInstance unit that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

5.1.5 As regard to **Claim 5**, this claim is drawn to the circuit simulating apparatus according to claim 1, wherein:

- said designating unit includes a circuit switching element specifying unit specifying a circuit switching element; **and**

- said circuit disconnecting unit forms a netlist with the portion of the circuit that will be ignored disconnected from the netlist extracted by said netlist extracting unit, based on the circuit switching element specified by said circuit switching element specifying unit.

Weber teaches [**Col 6, line 56 – Col 7 line 35**] a routine for:

- detecting the hspLoad property and generating a load circuit creating a load circuit; **and**
- forming a netlist with the portion of the circuit that will be ignored disconnected from the original netlist, based on the load circuit element specified by said switching element specifying unit.

5.1.6 As regard to **Claim 6**, this claim is drawn to the circuit simulating apparatus according to claim 5, further comprising a circuit recognizing unit recognizing whether the circuit disconnecting terminal connected to the circuit switching element specified by said circuit switching element specifying unit is on the main circuit side or the portion of the circuit that will be ignored side; wherein said circuit disconnecting unit adds a description for connecting the circuit switching terminal recognized to be on the portion of the circuit that will be ignored side by said circuit recognizing unit to a power supply or the ground, and adds a description for disconnecting connection with said portion of the circuit that will be ignored, on the netlist extracted by said netlist extracting unit.

Weber teaches [**Fig 9 and corresponding text**] a PrintInstance unit that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

5.1.7 As regard to **Claim 7**, this claim is drawn to the circuit simulating apparatus according to claim 5, further comprising a circuit recognizing unit for recognizing whether the circuit disconnecting terminal designated by said circuit disconnecting terminal designating unit is on the main circuit side or on the portion of the circuit that will be ignored; wherein said circuit disconnecting unit; adds a description for disconnecting connection between the circuit disconnecting terminal on the main circuit side with the circuit switching element on the netlist extracted by said extracting unit, when the circuit disconnecting terminal recognized to be on the side of the main circuit by said circuit recognizing unit is connected to a plurality of elements of the main circuit.

Weber teaches [**Fig 9 and corresponding text**] a PrintInstance unit that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

5.1.8 As regard to **Claim 8**, this claim is drawn to a method of circuit simulation, analyzing a circuitry having a main circuit and a portion of the circuit that will be ignored connected by a circuit switching element, comprising the steps of:

- extracting a netlist from circuit diagram data;

- designating an element between the main circuit and the portion of the circuit that will be ignored;
- forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist, based on said designated element;
- forming a simulation input file with reference to said formed netlist, a model parameter and an analysis condition; **and**
- performing a circuit simulation using said formed simulation input file.

Weber teaches **[Fig 7 and corresponding text]** the general steps of a method for simulating a portion of a circuit design connected to a main circuit by a circuit switching element, comprising the steps of:

- extracting a netlist from circuit diagram data **[Col 3, lines 45 – 67]**;
- designating an element between the main circuit and the portion of the circuit that will be ignored **[Col 6, lines 53 –67]**;
- forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist, based on said designated element **[Col 6, lines 45 –67]**;
- forming a simulation input file with reference to said formed netlist, a model parameter and an analysis condition **[Col 4, lines 50 – 64]**; **and**
- performing a circuit simulation using said formed simulation input file **[Col 3, lines 45 –49]**.

5.1.9 As regard to **Claim 9**, is drawn to method of circuit simulation according to claim 8, wherein

- said step of designating an element between said main circuit and the portion of the circuit that will be ignored includes the step of designating an circuit disconnecting terminal; **and**
- said step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist includes the step of forming a netlist with the portion of the circuit that will be ignored circuit disconnected from said extracted netlist, based on said designated circuit disconnecting terminal.

Weber teaches **[Col 3, lines 23 – 32]** the use of the "hspLoad" directive as an indicator for ignoring a portion of a circuit; and the HNL netlister **[Col 3, lines 45 – 65]**.

5.1.10 As regard to **Claim 10**, this claim is drawn to the method of circuit simulation according to claim 9 further comprising the step of recognizing whether said designated circuit disconnecting terminal is on the main circuit side or on the portion of the circuit that will be ignored side; wherein said step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist includes the step of adding a description for connecting the circuit disconnecting terminal recognized to be on the portion of the circuit that will be ignored side to a power supply or to the ground, and adding a description for disconnecting connection with said portion of the circuit that will be ignored, on said extracted netlist.

Weber teaches **[Fig 9 and corresponding text]** a PrintInstance unit that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

5.1.11 As regard to **Claim 11**, this claim is drawn to the method of circuit simulation according to claim 9, further comprising the step of recognizing whether said designated circuit disconnecting terminal is on the main circuit side or on the portion of the circuit that will be ignored side; wherein said step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist includes the step of adding a description for disconnecting connection of the circuit disconnecting terminal on the main circuit side and the circuit switching element, on said extracted netlist, when the circuit disconnecting terminal recognized to be on the main circuit side is connected to a plurality of elements of the main circuit.

Weber teaches **[Fig 9 and corresponding text]** a PrintInstance unit that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

5.1.12 As regard to **Claim 12**, this claim is drawn to the method of circuit simulation according to claim 8, wherein said step of designating an element between said main circuit and the portion of the circuit that will be ignored includes the step of specifying a circuit switching element; and said step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist includes the

step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist, based on said specified circuit switching element.

Weber teaches **[Col 6, line 56 – Col 7 line 35]** a routine for:

- detecting the hspLoad property and generating a load circuit creating a load circuit; **and**
- forming a netlist with the portion of the circuit that will be ignored disconnected from the original netlist, based on the load circuit element specified by said switching element specifying unit.

5.1.13 As regard to **Claim 13**, this claim is drawn to the method of circuit simulation according to claim 12, further comprising the step of recognizing whether the circuit disconnecting terminal connected to said specified circuit switching element is on the main circuit side or on the portion of the circuit that will be ignored side; wherein said step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist includes the step of adding a description for connecting the circuit disconnecting terminal recognized to be on the portion of the circuit that will be ignored side to a power supply or to the ground, and adding a description for disconnecting connection with said portion of the circuit that will be ignored, on said extracted netlist.

Weber teaches **[Fig 9 and corresponding text]** a PrintInstance unit that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

5.1.14 As regard to **Claim 14**, this claim is drawn to the method of circuit simulation according to claim 12, further comprising the step of recognizing whether said circuit disconnecting terminal connected to said specified circuit switching element is on the main circuit side or on the portion of the circuit that will be ignored side; wherein said step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist includes the step of adding a description for disconnecting connection between circuit disconnecting terminal on the main circuit side and circuit switching element, on said extracted netlist, when the circuit disconnecting terminal recognized to be on the main circuit side is connected to a plurality of elements of the main circuit.

Weber teaches **[Fig 9 and corresponding text]** a PrintInstance unit that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

5.1.15 As regard to **Claim 15**, this claim is drawn to a computer readable recording medium recording a program to have a computer execute a method of circuit simulation analyzing a circuitry having a main circuit and a portion of a circuit that will be ignored connected by a circuit switching element, wherein said method of circuit simulation including the steps of:

- extracting a netlist from circuit diagram data;

- designating an element between the main circuit and the portion of the circuit that will be ignored;
- forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist, based on said designated element;
- forming a simulation input file with reference: to said formed netlist, a model parameter and an analysis condition; **and**
- performing a circuit simulation using said formed simulation input file.

Weber teaches a computer readable medium having computer readable program code, when executed, implementing on a computer a method the for simulating a portion of a circuit design connected to a main circuit by a circuit switching element, including the steps of:

- extracting a netlist from circuit diagram data [**Col 3, lines 45 – 67**];
- designating an element between the main circuit and the portion of the circuit that will be ignored [**Col 6, lines 53 –67**];
- forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist, based on said designated element [**Col 6, lines 45 –67**];
- forming a simulation input file with reference to said formed netlist, a model parameter and an analysis condition [**Col 4, lines 50 – 64**]; **and**
- performing a circuit simulation using said formed simulation input file [**Col 3, lines 45 –49**].

5.1.16 As regard to **Claim 16**, this claim is drawn to the computer readable recording medium according to claim 15, wherein said step of designating an element between said main circuit and the portion of the circuit that will be ignored includes the step of designating an circuit disconnecting terminal; and said step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist includes the step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist, based on said designated circuit disconnecting terminal.

Weber teaches **[Col 3, lines 23 – 32]** a subroutine that uses the "hspLoad" directive as an indicator for ignoring a portion of a circuit; and the HNL netlister **[Col 3, lines 45 – 65]**.

5.1.17 As regard to **Claim 17**, this claim is drawn to the computer readable recording medium according to claim 16, wherein said method of circuit simulation further includes the step of recognizing whether said designated circuit disconnecting terminal is on the main circuit side or on the portion of the circuit that will be ignored side; and said step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist includes the step of adding a description for connecting the circuit disconnecting terminal recognized to be on the portion of the circuit that will be ignored side to a power supply or to the ground, and adding a description for disconnecting connection with said portion of the circuit that will be ignored, on said extracted netlist.

Weber teaches **[Fig 9 and corresponding text]** a PrintInstance subroutine that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

5.1.18 As regard to **Claim 18**, this claim is drawn to the computer readable recording medium according to claim 16, wherein said method of circuit simulation further includes the step of recognizing whether said designated circuit disconnecting terminal is on the main circuit side or on the portion of the circuit that will be ignored side; and said step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist includes the step of adding a description for disconnecting connection of the circuit disconnecting terminal on the main circuit side and the circuit switching element, on said extracted netlist, when the circuit disconnecting terminal recognized to be on the main circuit side is connected to a plurality of elements of the main circuit.

Weber teaches **[Fig 9 and corresponding text]** a PrintInstance subroutine that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

5.1.19 As regard to **Claim 19**, this claim is drawn to the computer readable recording medium according to claim 15, wherein said step of designating an element between said main circuit and the portion of the circuit that will be ignored includes the step of specifying a circuit switching element; and said step of forming a netlist with the

portion of the circuit that will be ignored disconnected from said extracted netlist includes the step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist, based on said specified circuit switching element.

Weber teaches **[Col 6, line 56 – Col 7 line 35]** a routine for:

- detecting the hspLoad property and generating a load circuit creating a load circuit; **and**
- forming a netlist with the portion of the circuit that will be ignored disconnected from the original netlist, based on the load circuit element specified by said switching element specifying unit.

5.1.20 As regard to **Claim 20**, this claim is drawn to a computer readable recording medium according to claim 19, wherein said method of circuit simulation further includes the step of recognizing whether the circuit disconnecting terminal connected to said specified circuit switching element is on the main circuit side or on the portion of the circuit that will be ignored side; and said step of forming a netlist with the portion of the circuit that will be ignored disconnected from said extracted netlist includes the step of adding a description for connecting the circuit disconnecting terminal recognized to be on the portion of the circuit that will be ignored side to a power supply or to the ground, and adding a description for disconnecting connection with said portion of the circuit that will be ignored, on said extracted netlist.

Weber teaches **[Fig 9 and corresponding text]** a PrintInstance unit that uses a property list or other directive for connecting a power supply device to the circuit disconnecting terminal and adding a description to the netlist.

Additional references

6. The following is a list of references that are relevant to the claimed invention but were not cited by the examiner:

- US Patent No. 6,311,309 issued to Timothy J. Southgate
- US Patent No. 5,867,399 issued to Rostoker et al.
- US Patent No. 6,374,205 issued to Kuribayashi et al.
- US Patent No. 5,416,717 issued to Miyama et al.
- P.M. Maurer; "Efficient Simulation for Hierarchical and Partitioned Circuits"; VLSI Design 1999; Proc. 12th Int. Conf. 7 –10 Jan 1999; Pgs 236-241

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Morella Rosales-Hanner whose telephone number is (703) 305-8883. The examiner can normally be reached Monday-Friday from 7:00 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 703 308-6647. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MRH

Sep. 14th, 2004

JEAN R. HOMERE
PRIMARY EXAMINER